Appln. No. 10/606,872
Reply to Office Action Mailed October 21, 2005

Amendments to the Specification:

Please replace paragraph [0058] with the following amended paragraph:

While up and running, Step 116, if a change in value on the SPD_SEL BUS is detected, as by insertion of an illegal memory board 22_{n+1} (FIG. 9) Step 118, an interrupt is sent to the directors 24_1-24_M, Step 120; otherwise the system remains running, Step 116. If an interrupt is sent, Step 120, a determination is made as to whether there is a logic 00 condition on the SPD_SEL BUS, Step 122. If a logic 00 condition is detected in Step 122, software sends an error message to the directors 24_1-24_M, Step 138. In response to such error message, the decoders 54 will allow the SERDES sd1-sd7, which are coupled to the legal memory boards 22_1-22_n in FIG. 9 to remain operational. However, in response to the error message, the directors 24_1-24_M with have the decoders 54 thereof disable the SERDES sd8 coupled to the newly inserted, albeit illegal memory board, here in this example in FIG. 9, the memory board 22_{n+1}. Thus, in this example, SERDES sd8 of all director boards 24_1-24_M will be disabled via EN8 signal. Otherwise, if in Step 122 the is no 00 logic condition detected on the SPD_SEL BUS in Step 122, a determination is made as to whether there is a logic 10 or 11 condition on the SPD_SEL BUS, Step 124. If there is neither logic condition, the system is set to low speed and software enables the gates (i.e., ports) from/to the memory boards detected to be on the backplane, Step 126. On the other hand, if in Step 124 there is either a logic 10 or 11 condition on the SPD_SEL BUS, the system is set to the high speed and software enables the gates (i.e., ports) from/to the memory boards detected to be on the backplane, Step 128. In both cases, i.e., Step 126 or Step 128, the system is up and running, Step 116.